Remarks

This amendment is submitted with a Request for Continued Examination (RCE), in response to the Office Action mailed November 2, 2006. Claims 1 – 38 are pending in the application. Claims 1 – 26 are rejected. In this amendment, the Applicants have canceled claims 7, 15, 17, 19 and 27 - 30.

The Applicants have added new dependent claims 31 – 38. These new claims represent subject matter to which the Applicants believe they are entitled to claim. Each of the new claims is supported by the specification including the drawings. The Applicants respectfully request reconsideration of the present application in view of the remarks set forth below.

Claim Rejections – 35 U.S.C § 112

Claims 1 – 26 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Specifically, the Examiner states that the phrase "whether or not a neighboring processor node comprises another software extensible device" in independent claims 1 and 18 rendered the claims indefinite, as it is unclear as to whether or not the neighboring processor node is one of a plurality of previously mentioned "plurality of processing nodes."

Independent claims 1 and 18 are currently amended to overcome the Examiner's rejection. Dependent claims 2 – 6, 8 – 14, 16, and 20 – 26 overcome the Examiner's rejections for at least the same reasons as independent claims 1 and 18, from which they depend.

Claim Rejections – 35 U.S.C § 103

Claims 1 – 26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Willis et al., U.S. Patent No. 5,999,734 (hereinafter Willis) in view of Arimilli et al., U.S. Patent No. 6,415,424 (hereinafter Arimilli).

Regarding independent claim 1, the Applicants have amended claim 1 to recite, in part:

> a first communication interface including a first array interface module configured to interface to a first other member of the plurality of processor nodes, and a first standard input/output interface configured to communicate with a first input/output device,
>
> a second communication interface including a second array interface module configured to interface to a second other member of the plurality of processor nodes, and a second standard input/output interface configured to communicate with a second input/output device;

Willis teaches "a hardware apparatus consisting of shared memory multiprocessors optionally augmented by processors with reconfigurable logic execution pipelines" (Abstract). The reconfigurable logic blocks (FIG. 1, component 9) in Willis are coupled using shared resources, i.e., a "shared memory interconnect" (FIG. 1, component 7), and a single "message interconnect" (FIG. 1, component 13). A shared resource, such as those taught in Willis, does not provide the performance advantages of a dedicated resource used to communicate between processor elements. Thus, Willis does not teach or suggest the limitations recited in amended claim 1, for example, "first array interface module configured to *interface to a first other member of the plurality of processor nodes*" and "a second array interface module configured to *interface to a second other member of the plurality of processor nodes*" (emphasis added).

Arimilli teaches that a "processor chip is interconnected to the external components via point-to-point bus connections controlled by an integrated distributed switch (IDS) controller." (Abstract). Arimilli further teaches a multiprocessor chip having a single, shared switch coupling the processor elements (FIG. 2B, components 166 and 160A-D). The switches disclosed in Arimilli do not provide the performance advantages of one or more dedicated resources used to communicate to external components or to communicate between processor elements. Thus, Arimilli does not teach or suggest the limitations recited in amended claim 1, for example, "first array interface module configured to *interface to a first other member of the plurality of processor nodes*" and "a second array interface module configured to *interface to a second other member of the plurality of processor nodes*" (emphasis added). For these reasons, the Applicants believe that claim 1, and those claims that depend from claim 1, should be allowed.

Regarding dependent claims 2 – 6, 8 – 14, 16, and 31 – 36, the Applicants believe that these claims are allowable for at least the same reasons discussed herein with regard to claim 1, from which claims 2 – 6, 8 – 14, 16, and 31 - 36 depend.

Regarding independent claim 18, the Applicants have amended claim 18 to recite, in part,

> communicating using a first communication interface including a first array interface module configured to interface to a first other member of the plurality of processing nodes;
>
> determining if a neighboring device is a member of the plurality of processor nodes;
>
> if the neighboring device is a member of the plurality of processing nodes, communicating to the neighboring device using a second communication interface including a second array interface module; and

if the neighboring device is not a member of the plurality of processing nodes, communicating to the neighboring device using a standard input/output interface of the second communication interface.

As discussed herein, Willis teaches reconfigurable logic blocks (FIG. 1, component 9) communicating using shared resources, i.e., a "shared memory interconnect" (FIG. 1, component 7), and a single "message interconnect" (FIG. 1, component 13). Thus, the communications between the reconfigurable logic blocks disclosed in Willis use shared resources. A shared resource, such as that taught in Willis, does not provide the performance advantages of a dedicated resource used to communicate between processor elements. Thus, Willis does not teach or suggest the limitations recited in amended claim 18, including "communicating using a first communication interface including a first array interface module configured to *interface to a first other member of the plurality of processing nodes*" and, if a neighboring device is a member of the plurality of processor nodes, "*communicating to the neighboring device using a second communication interface including a second array interface module*" (emphasis added).

For at least the same reasons discussed with respect to claim 18 and Willis, the single, shared switch taught in Arimilli (FIG. 2B, component 166) does not provide the performance advantages of a dedicated resource used to communicate between processor elements. Thus, Arimilli does not teach or suggest the limitations recited in amended claim 18. For these reasons, the Applicants believe that independent claim 18 should be allowed.

Regarding dependent claims 20 – 26, 37 and 38, the Applicants believe that these claims are allowable for at least the same reasons discussed herein with regard to claim 18, from which claims 20 – 26, 37 and 38 depend.

Conclusion

The Applicants believe that all pending claims are allowable and respectfully request that the Examiner issue a Notice of Allowance. The Examiner is invited to contact the Applicants' undersigned representative with any questions concerning the present application.

Respectfully submitted,

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